**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Patent Application**

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| Applicant(s): | Fischer et al. |
| Case: | 46-3 |
| Serial No.: | 10/719,645 |
| Filing Date: | November 21, 2003 |
| Group: | 2627 |
| Examiner: | Dismery E. Mercedes |
| Title: | Long Hold Time Sample and Hold Circuits |

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REPLY BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants hereby reply to the Examiner's Answer, mailed July 24, 2007 (referred to hereinafter as "the Examiner's Answer"), in an Appeal of the final rejection of claims 1-20 in the above-identified patent application.

REAL PARTY IN INTEREST

A statement identifying the real party in interest is contained in Appellants' Appeal Brief.

RELATED APPEALS AND INTERFERENCES

A statement identifying related appeals is contained in Appellants' Appeal Brief.

## STATUS OF CLAIMS

A statement identifying the status of the claims is contained in Appellants' Appeal Brief.

## STATUS OF AMENDMENTS

A statement identifying the status of the amendments is contained in Appellants' Appeal Brief

## SUMMARY OF CLAIMED SUBJECT MATTER

A Summary of the Invention is contained in Appellants' Appeal Brief.

## STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A statement identifying the grounds of rejection to be reviewed on appeal is contained in Appellants' Appeal Brief

## CLAIMS APPEALED

A copy of the appealed claims is contained in an Appendix of Appellants' Appeal Brief

## ARGUMENT

Independent Claims 1 and 8

Independent claims 1 and 8 are rejected under 35 U.S.C. §102(e) as being anticipated by Luo. In particular, the Examiner asserts that Luo discloses a sample and hold circuit. Among other features, the Examiner asserts that Luo also discloses (i) at least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output (citing element C1 in FIG. 1); (ii) at least one output switch for selectively connecting said at least one capacitive element to said output (citing element S3 of FIG. 1); and (iii) an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches

is limited to said offset voltage (FIG. 1: element 11; col. 3, lines 50-64).

Applicants note that, regarding element C1, Luo teaches that,

> continuing to refer to FIG. 1 and FIG. 2, **during quarter period 2** switch S1 connecting the first transconductor 10 to the operational amplifier 11 is open, and switch S2 connecting the sample and hold capacitor C2 to the output of the operational amplifier 11 is closed allowing capacitor C2 to be charged up to a voltage equal to that on capacitor C1. **Switches S4a and S4b remain closed.** Switch S6 is closed to discharge the voltage on the parasitic capacitance at the output of the transconductor 10. **All other switches are open during quarter period 2.**
>
> Continuing to refer to FIG. 1 and FIG. 2, **during quarter period 3** switch S0 is closed to discharge the voltage on the feed back capacitor C1. Switch S5a is closed to connect input voltage $k_2$ $V_R$ to the input of the transconductor 10 and **switch S5b is closed to connect a voltage reference $-V_R$ to the (+) input terminal of the current summing operational amplifier 11**. Switch S6 remains closed to discharge the voltage on the parasitic capacitance at the output of the transconductor 10. **All other switches are open during quarter period 3.**
>
> Continuing to refer to FIG. 1 and FIG 2, during quarter periods 4 and 5 switches S1, S5a and S5b are closed, and all other switches are open. The feedback capacitor C1 is charged for one half clock period by the output of the transconductor 10 from the reference voltage $-V_R$ to a voltage $-V_y$. During quarter period 6 switches S5a and S5b remain closed and S3 is closed allowing a voltage equal to that on capacitor C1 to be put onto capacitor C3. Switch S6 is closed to discharge the capacitance on the parasitic capacitance at the output of the transconductor 10, and all other switches are open.
> (Col 4, lines 23-53; emphasis added.)

Luo teaches that *switch S4b is closed and switch S5b is open during quarter 2*, and that *switch S4b is open and switch S5b is closed during quarter 3*. Thus, Luo actually *teaches away* from the present invention by teaching to ***not*** *limit* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*. Independent claim 1 requires an amplifier connected to said node, *wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage*. Independent claim 8 requires *limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element*.

Thus, Luo does not disclose or suggest an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of

said input and output switches is limited to said offset voltage, as required by independent claim 1, and does not disclose or suggest limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element, as required by independent claim 8.

Claims 4 and 11

Claims 4 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Luo in view of Beauducel et al. Regarding claims 4 and 11, the Examiner acknowledges that Luo does not explicitly teach the limitation of claims 4 and 11, but asserts that Beauducel teaches two switches found between the input and output nodes in order to hold a voltage amount (col. 3, lines 1-20).

Applicants note, however, that neither Luo nor Beauducel disclose or suggest wherein switches selectively connect at least one input and output switches *to an output of an amplifier in a hold mode or standard voltages in a write mode to reduce leakage effects* due to parasitic diodes in the input and output switches. Claims 4 and 11 require wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in a hold mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches.

Thus, Luo and Beauducel, alone or in combination, do not disclose or suggest wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in a hold mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches, as required by claims 4 and 11.

Claims 7 and 13

Claims 7 and 13 are rejected under 35 U.S.C. §102(e) as being anticipated by Luo. Regarding claims 7 and 13, the Examiner asserts that "it is inherent that because the voltage drop cannot be greater than the voltage offset, hence it reduces the leakage effect in the circuit by maintaining the voltage offset during the operation of the circuit."

Applicants note that, as argued above, Luo does *not* teach *to limit* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected*

*to the capacitive element*. Furthermore, Luo does *not* disclose or suggest wherein the limited voltage drop across at least one of the input and output switches *reduces a leakage of the sample and hold circuit*. Claims 7 and 13 require wherein said limited voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit.

Thus, Luo does not disclose or suggest wherein said limited voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit, as required by claims 7 and 13.

Additional Cited References

Beauducel was also cited by the Examiner for its disclosure of a resistor placed in parallel as disclosed in the sample and hold circuit of FIG. 4 ($R_1$). Although Beauducel is directed to a sample and hold circuit, Beauducel does *not* disclose or suggest the feature of *limiting* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*.

Thus, Beauducel et al. do not disclose or suggest an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, as required by independent claim 1, and do not disclose or suggest limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element, as required by independent claim 8.

Mills was also cited by the Examiner for its disclosure of a sample and hold circuit in which its hold time is 200 microseconds. Applicants note that Mills is directed to an analog to digital signal converter that includes an integrator and a sample and hold circuit. Mills does *not*, however, disclose or suggest the feature of *limiting* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*.

Thus, Mills et al. do not disclose or suggest an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, as required by independent claim 1, and do not disclose or suggest limiting a voltage drop across at least one of said input and

output switches to an offset voltage of an amplifier connected to said at least one capacitive element, as required by independent claim 8

Sandusky was also cited by the Examiner for its disclosure of a sample and hold circuit for a preamplifier in a disk drive Applicants note that Sandusky is directed to a circuit for input switching for a read channel Sandusky does *not*, however, disclose or suggest the feature of *limiting* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*

Thus, Sandusky et al. do not disclose or suggest an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, as required by independent claim 1, and do not disclose or suggest limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element, as required by independent claim 8.

Conclusion

The rejections of the cited claims under sections 102 and 103 in view of Luo, Beauducel et al , Mills et al. and Sandusky et al , alone or in combination, are therefore believed to be improper and should be withdrawn The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

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Date: September 24, 2007

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## APPENDIX

1. A sample and hold circuit having an input and an output, comprising:

at least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output;

at least one input switch for selectively connecting said at least one capacitive element to said input;

at least one output switch for selectively connecting said at least one capacitive element to said output; and

an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage.

2. The sample and hold circuit of claim 1, wherein said sample and hold circuit is part of a preamplifier for a head bias circuit in a storage system.

3. The sample and hold circuit of claim 1, wherein at least one of said input and output switches has a leakage effect represented by a resistor in parallel with said input or output switch and a voltage drop across said resistor is limited to said offset voltage.

4. The sample and hold circuit of claim 1, further comprising at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in a hold mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches.

5. The sample and hold circuit of claim 1, wherein said output provides a DC bias for a magneto-resistive head in a disk drive.

6. The sample and hold circuit of claim 1, wherein said sample and hold circuit provides a hold time of at least approximately 200 microseconds

7 The sample and hold circuit of claim 1, wherein said limited voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit.

8. A method for reducing leakage in a sample and hold circuit having at least one capacitive element for retaining a charge, said method comprising the steps of:

configuring at least one input switch to selectively connect said at least one capacitive element to said input;

configuring at least one output switch to selectively connect said at least one capacitive element to said output; and

limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element.

9. The method of claim 8, wherein said sample and hold circuit is part of a preamplifier for a head bias circuit in a storage system.

10. The method of claim 8, wherein at least one of said input and output switches has a leakage effect represented by a resistor in parallel with said input or output switch and a voltage drop across said resistor is limited to said offset voltage.

11. The method of claim 8, further comprising the steps of configuring at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in a hold mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches.

12. The method of claim 8, wherein said sample and hold circuit provides a hold time of at least approximately 200 microseconds.

13. The method of claim 8, wherein said step of limiting a voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit.

14. A disk drive, comprising:

a magneto-resistive read head; and

a sample and hold circuit having an input and an output, comprising:

(i) at least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output;

(ii) at least one input switch for selectively connecting said at least one capacitive element to said input;

(iii) at least one output switch for selectively connecting said at least one capacitive element to said output; and

(iv) an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage.

15. The disk drive of claim 14, wherein said sample and hold circuit is part of a preamplifier for a head bias circuit in a storage system.

16. The disk drive of claim 14, wherein at least one of said input and output switches has a leakage effect represented by a resistor in parallel with said input or output switch and a voltage drop across said resistor is limited to said offset voltage.

17. The disk drive of claim 14, further comprising at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in a hold

mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches.

18. The disk drive of claim 14, wherein said output provides a DC bias for a magneto-resistive head in said disk drive.

19. The disk drive of claim 14, wherein said sample and hold circuit provides a hold time of at least approximately 200 microseconds.

20. The disk drive of claim 14, wherein said limited voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit

## EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.